Subject : Computer Organization and Architecture

Day : Wednesday   **S.D.E.** ‖‖‖‖‖‖‖‖   Time : 10.00 A.M. TO 1.00 P.M.

Date : 07/12/2016   **33515**   Max Marks : 80   Total Pages : 1

N.B.:

1) Solve any **FIVE** questions from Section-I and any **TWO** questions from Section-II.
2) Both the sections should be written in the **SAME** answer book.
3) Figures to the **RIGHT** indicate full marks.

SECTION-I

Q.1 Explain the functioning of binary counter with help of logic circuit in detail. **(10)**

Q.2 Explain the terms: **(10)**
 a) Register transfer
 b) Shift register
 c) Logic gates

Q.3 Describe DMA transfer in detail. **(10)**

Q.4 Discuss various types of mapping techniques associated with cache memory with their merits and demerits. **(10)**

Q.5 Explain interrupt cycle with help of flow chart. **(10)**

Q.6 Differentiate between: **(10)**
 a) Hardwired control unit and Micro-programmed control unit.
 b) Synchronous data transfer and Asynchronous data transfer.

Q.7 Write short notes on any **TWO** of the following: **(10)**
 a) Stack organization
 b) Half adder
 c) Multiplication algorithm

SECTION-II

Q.8 a) Simplify the following with K map. **(10)**
 i) $F(x, y, z) = \Sigma (0, 2, 3, 4, 6)$
 ii) $F(a, b, c, d) = \Sigma (0, 1, 2, 4, 5, 7, 11, 15)$.

 b) Show that J and K flip-flop can be converted to D flip-flop with an inverter between J and K inputs. **(05)**

Q.9 A sequential circuit has two D flip flops A and B, one inputs x and one output z. The flip-flop input equations and circuit outputs are as follows: **(15)**
 $D_A = Ax + Bx$
 $D_B = A'x'$
 $z = Ax + B'x$
 a) Draw the logic diagrams of the circuit.
 b) Tabulate the state table.

Q.10 a) Solve the following: **(10)**
 i) Find 2' complement of 1101110.
 ii) $1111001 - 0011011$
 iii) $101101 * 110$

 b) Give the CISC characteristics. **(05)**

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